AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of generating a program trace on a multithreaded processor, the method comprising:

detecting issuance of a first instruction;

generating a first program trace entry for the first instruction, wherein the first program trace entry includes a first thread ID for the first instruction;

detecting issuance of a second instruction;

generating a second program trace entry for the second instruction, wherein the second program trace entry includes a second thread ID for the second instruction, ~~; and~~ wherein the first thread ID is different than the second thread ID;

detecting the occurrence of a thread switch; and

performing a synchronization operation in response to the thread switch, wherein the synchronization operation comprises inserting a number equal to the number of instructions issued since a previous synchronization operation into the program trace.

2-3 (Canceled)

4. (Original) The method of claim 2, wherein the synchronization operation further comprises inserting a program counter into the program trace.

5. (Original) The method of claim 1, further comprising compressing the program trace.

6. (Original) The method of claim 5, wherein the compressing the program trace comprises tokenizing the first program trace entry and the second program trace entry.

7. (Original) The method of claim 1, further comprising periodically performing synchronization operations with the program trace.

8. (Currently Amended) A program trace generator for generating a program trace on a multithreaded processor comprising:

means for detecting issuance of a first instruction;

means for generating a first program trace entry for the first instruction, wherein the first program trace entry includes a first thread ID for the first instruction;

means for detecting issuance of a second instruction;

means for generating a second program trace entry for the second instruction, wherein the second program trace entry includes a second thread ID for the second instruction~~; and,~~ wherein the first thread ID is different than the second thread ID;

means for detecting the occurrence of a thread switch; and

means for performing a synchronization operation in response to the thread switch, wherein the means for performing a synchronization operation comprises means for inserting a number equal to the number of instructions issued since a previous synchronization operation into the program trace.

9-10. (Canceled)

11. (Original) The program trace generator of claim 9, wherein the means for performing a synchronization operation further comprises means for inserting a program counter into the program trace.

12. (Original) The program trace generator of claim 8, further comprising means for compressing the program trace.

13. (Original) The program trace generator of claim 12, wherein the means for compressing the program trace comprises means for tokenizing the first program trace entry and the second program trace entry.

14. (Original) The program trace generator of claim 8, further comprising means for periodically performing synchronization operations with the program trace.

15. (Original) A method of generating a program trace on a multithreaded processor, the method comprising:

detecting issuance of a first instruction;

generating a first program trace entry for the first instruction;

detecting a thread switch; and

inserting a thread switch marker into the program trace when a thread switch is detected.

16. (Original) The method of claim 15, further comprising:

detecting issuance of a second instruction; and

generating a second program trace entry for the first instruction.

17. (Original) The method of claim 16, wherein the first instruction is from first thread and the second instruction is from a second thread.

18. (Original) The method of claim 15, further comprising compressing the program trace.

19. (Original) The method of claim 18, wherein the compressing the program trace comprises:

tokenizing the first program trace entry to form a first program trace token; and

tokenizing the thread switch marker into a thread switch token.

20. (Original) The method of claim 15, further comprising periodically performing synchronization operations with the program trace.

21. (Original) The method of claim 20, wherein the synchronization operation further comprises inserting a program counter into the program trace.

22. (Original) The method of claim 15, wherein the thread switch marker contains a first thread ID of the active thread after the thread switch.

23. (Original) The method of claim 22, wherein the thread switch marker contains a second thread ID of the active thread before the thread switch.

24. (Original) A program trace generator for generating a program trace on a multithreaded processor, the program trace generator comprising:

means for detecting issuance of a first instruction;

means for generating a first program trace entry for the first instruction;

means for detecting a thread switch; and

means for inserting a thread switch marker into the program trace when a thread switch is detected.

25. (Original) The program trace generator of claim 24, further comprising:

means for detecting issuance of a second instruction; and

means for generating a second program trace entry for the first instruction.

26. (Original) The program trace generator of claim 25, wherein the first instruction is from first thread and the second instruction is from a second thread.

27. (Original) The program trace generator of claim 24, further comprising means for compressing the program trace.

28. (Original) The program trace generator of claim 27, wherein the means for compressing the program trace comprises:

means for tokenizing the first program trace entry to form a first program trace token; and

means for tokenizing the thread switch marker into a thread switch token.

29. (Original) The program trace generator of claim 24, further comprising means for periodically performing synchronization operations with the program trace.

30. (Original) The program trace generator of claim 29, wherein the means for performing a synchronization operation further comprises means for inserting a program counter into the program trace.

31. (Original) The program trace generator of claim 24, wherein the thread switch marker contains a first thread ID of the active thread after the thread switch.

32. (Original) The program trace generator of claim 31, wherein the thread switch marker contains a second thread ID of the active thread before the thread switch.

33. (New) A program trace generator for generating a program trace on a multithreaded processor comprising:

detector configured to detect issuance of a first instruction;

generator configured to generate a first program trace entry for the first instruction, wherein the first program trace entry includes a first thread ID for the first instruction;

detector configured to detect issuance of a second instruction;

generator configured to generate a second program trace entry for the second instruction, wherein the second program trace entry includes a second thread ID for the second instruction, wherein the first thread ID is different than the second thread ID;

detector configured to detect the occurrence of a thread switch; and

performer configured to perform a synchronization operation in response to the thread switch, wherein the performer comprises inserter configured to insert a number equal to the number of instructions issued since a previous synchronization operation into the program trace.

34. (New) A program trace generator for generating a program trace on a multithreaded processor, the program trace generator comprising:

detector configured to detect issuance of a first instruction;

generator configured to generate a first program trace entry for the first instruction;

detector configured to detect a thread switch; and

inserter configured to insert a thread switch marker into the program trace when a thread switch is detected.